ABSTRACT OF THE DISCLOSURE

To provide a semiconductor integrated circuit device that reduces charging and discharging currents flowing through clock tree synthesis, thereby reducing current consumption of entire circuits of the semiconductor integrated circuit device.

In a semiconductor integrated circuit device including a clock synchronous type circuit that operates in synchronization with either of rising and falling edges flank of a reference clock and a plurality of clock buffer circuits for distributing the reference clock to the clock synchronous type circuit, each clock buffer circuit is constituted from a first transistor that drives a load at one of the edges flank of the reference clock with which the clock synchronous type circuit does not operate in synchronization and a second transistor that drives the load at the other edge flank of the reference clock. A gate width of the first transistor is set so that a change in the edge flank is slowed down, provided that a pulse waveform of the reference clock is not destroyed. A carrier type of the second transistor is different from the carrier type of the first transistor, and the second transistor is formed to have the gate width larger than the first transistor.